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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/542,727

07/20/2005

Takayuki Noto

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10/27/2006

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EXAMINER

TAN, VIBOL

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/542,727

Applicant(s)

NOTO ET AL.

Examiner

Vibol Tan

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2 and 4-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8 and 11 is/are rejected.
- 7) ☒ Claim(s) 9-10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 4-8 are objected to because of the following informalities:

In claims 4-7, correct words resister and resisters to resistor and resistors.

In claim 8, line 3; change "the output signal" to "an output signal" to avoid lack of antecedent basis. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 4, 5 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 4, 5 and 11, the claimed recitation of "...an input impedance during input signal transition is lower than an input impedance on other occasions than input signal transition" is not clearly understood because of the following phrase "than input signal transition". It is further not clear whether the last cited input signal transition same or different from the previously cited input signal transition. Clarification is necessary in order for the claimed limitation to be properly interpreted.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Hojo et al. (U.S. Pat. 5,952,850).

In claim 1, Hojo et al. teaches all claimed features in Figs. 3 and 4, a semiconductor integrated circuit comprising: an input circuit (15) for taking in signals (from pad 5); and an output circuit (6) for outputting signals (to pad 5), wherein the input circuit (15) is so set that an input impedance (input impedance for 15 while taking or receiving signals from the pad 5) during input signal transition is lower (low impedance in order to accept signals) than an input impedance on other occasions (times when 15 not receiving or taking signals), and wherein the output circuit (6) is so set that a driving force (read as a logic level when the logic level changing its state; in this case the driving force is at logic 0 at terminal 1) during a second half of signal transition (when output circuit 6 outputs low signal level at pad 5) is lower than a driving force during (read as a logic level when the logic level changing its state; in this case the driving force is at logic 1 at terminal 3) a first half of transition (when output circuit 6 outputs high signal level at pad 5).

In claim 2, Hojo et al. further teaches the semiconductor integrated circuit according to claim 1, wherein the input circuit (15) and the output circuit (6) are connected in common to a pad (5) that enables inputting/outputting of signals.

6. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Flaherty (U.S. Pat. 4,855,623).

In claim 8, Flaherty teaches all claimed features in Fig. 1, a semiconductor integrated circuit comprising: an internal circuit (a circuit that supplies data 24; not shown); and an output circuit (10) that can externally output an output signal (data 24) of the internal circuit, wherein the output circuit comprises: a first output circuit (28, 36) that can drive an external load (a load couples to OUTPUT node 22; not shown) based on the output signal (data 24) of the internal circuit during a first half of transition (when enable 30 is placed at logic 1, output 22 assumes the same logical value as applied to the terminal data 24) of a signal to be outputted; and a second output circuit (20, 42) whose driving force is set lower (col. 4, lines, 31-41, Flaherty talks about when other ratios between two modes are desired, then the sizes of the driver transistors 28, 36 and 20, 42 can be tailored to provide the desired ratio; accordingly, the size ratios of transistors are directly related to driving force or strength of the transistors, thus the drive strength of 20, 42 can be set lower than the drive strength of 28, 36) than that of the first output circuit and which can drive the external load.

7. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 4, 5 and 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

9. Claims 6 and 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

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10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bedarida et al. (US 6,567,318) teaches control circuit for an output driving stage of an IC.

Casper (US 6,154,056) teaches tri-stating address input circuit.

Okumura (US 6,107,830) teaches IC device including CMOS tri-state drivers suitable for powerdown.

Bacigalupo (US 6,448,812) teaches pull-up/pull-down logic for holding a defined value during power down mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



**VIBOL TAN**  
**PRIMARY EXAMINER**